Hardik Sharma

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EDUCATION

Georgia Institute of Technology

PhD in Electrical and Computer Engineering | January 2016 - Present
Area | Computer Architecture
Advisor | Prof. Hadi Esmaeilzadeh
Topic | Accelerated Deep Learning for the Edge-to-Cloud Continuum

Georgia Institute of Technology

MS in Electrical and Computer Engineering | December 2015
Area | VLSI Systems and Digital Design
Advisor | Prof. Hadi Esmaeilzadeh
GPA | 4.0/4.0

Indian Institute of Technology, Guwahati

B.Tech. in Electronics and Communication Engineering | June 2013
GPA | 8.13/10.0

HONORS AND AWARDS

Qualcomm Innovation Fellowship, Qualcomm USA | 2018
Together with Mohammad Ghasemzadeh. 8 teams out of 174 nationwide

Distinguished Paper Award in IEEE Symposium on High Performance Computer Architecture | 2016
"TABLA: A Unified Template-based Framework for Accelerating Statistical Machine Learning"

PUBLICATIONS

Conference Papers

[P6] **H. Sharma**, J. Park, N. Suda, L. Lai, B. Chau, V. Chandra, H. Esmaeilzadeh, **"Bit Fusion: Bit-Level Dynamically Composable Architecture for Accelerating Deep Neural Networks,"** in The 45^{th} International Symposium on Computer Architecture (ISCA), June 2018

[P5] J. Park, **H. Sharma**, D. Mahajan, J. Kim, H. Esmaeilzadeh, **"Scale-Out Acceleration for Machine Learning,"** in The 50^{th} Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), October 2017

[P4] **H. Sharma**, J. Park, D. Mahajan, E. Amaro, J. Kim, C. Shao, A. Mishra, H. Esmaeilzadeh, **"From High-Level Deep Neural Models to FPGAs,"** in The 49^{th} Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2016. Artifact: http://www.act-lab.org/artifacts/dnnweaver

[P3] D. Mahajan, J. Park, E. Amaro, **H. Sharma**, A. Yazdanbakhsh, J. Kim, Hadi Esmaeilzadeh, **"TABLA: A Unified Template-based Framework for Accelerating Statistical Machine Learning,"** 22^{nd} IEEE Symposium on High Performance Computer Architecture (HPCA), March 2016. (Distinguished Paper Award)
Artifact: http://www.act-lab.org/artifacts/tabla

[P2] W. Wahby, T. Sarvey, **H. Sharma**, H. Esmaeilzadeh, M. Bakir, **"The Impact of 3D Stacking on GPU-Accelerated Deep Neural Networks: an Experimental Study,"** IEEE International 3D Systems Integration Conference (3DIC), 2016.

[P1] A. Yazdanbakhsh, J. Park, **H. Sharma**, P. Lotfi-Kamran, H. Esmaeilzadeh, **"Neural Acceleration for GPU Throughput Processors,"** 48^{th} International Symposium on Microarchitecture (MICRO), December 2015

Book Chapters

[B1] A. Yazdanbakhsh, J. Park, **H. Sharma**, P. Lotfi-Kamran, H. Esmaeilzadeh, **"Neural Acceleration for GPU Throughput Processors,"** Advances in GPU Research and Practice, Elsevier, 2016

Workshop Papers

[W2] **H. Sharma**, W. Wahby, T. Sarvey, M.S. Bakir, H. Esmaeilzadeh, **"Approximate Computing and Microfluidic Cooling for Enhanced Machine Learning,"** in Workshop on Approximate Computing (WAX) @ASPLOS, 2016

[W1] **H. Sharma**, J. Park, E. Amaro, B. Thwaites, P. Kotha, A. Gupta, J. Kim, A. Mishra, H. Esmaeilzadeh, **"DnnWeaver: From High-Level Deep Network Models to FPGA Acceleration",** in Workshop on Cognitive Architectures @ASPLOS, 2016

Technical Reports

[TR2] D. Mahajan, J. Park, E. Amaro, **H. Sharma**, A. Yazdanbakhsh, J. Kim, Hadi Esmaeilzadeh, **"TABLA: A Unified Template-based Framework for Accelerating Statistical Machine Learning,"** SMARTech, SCS Technical Report, GT-CS-15-07

[TR1] A. Yazdanbakhsh, J. Park, **H. Sharma**, P. Lotfi-Kamran, H. Esmaeilzadeh, **"Neural Acceleration for GPU Throughput Processors,"**SMARTech, SCS Technical Report, GT-CS-15-05

Poster Presentations

[PP2] **H. Sharma**, T. Olson, A. Chalfin, **"Using Texture Compression Hardware for Neural Network Inference,"** in Hot Chips: A Symposium on High Performance Chips, 2017

[PP1] **H. Sharma**, T. Olson, A. Chalfin, **"Compressing Deep Neural Networks with ASTC",** in High-Performance Graphics (HPG), 2017

PROFESSIONAL EXPERIENCE

ARM INC. | Research Intern — Summer 2017
Team: R&D ML-IoT, San Jose, CA
Mentor: Dr. Naveen Suda • Manager: Prof. Vikas Chandra

- Developed low-precision RNN and LSTMs models for Human Activity Recognition and Keyword-Spotting
- Developed a variable-precision architecture that dynamically composes bit-level compute units for accelerating CNNs/RNNs under strict power and area budgets

ARM INC. | Research Intern — Summer 2016
Teams: Media Processing Group (GPU Architecture) and R&D, San Jose, CA
Mentor: Alex Chalfin • Manager: Alpana Kaulgud

- Developed a compressed DNN training algorithm using ASTC Texture Compression
- Accelerated DNN inference for mobile GPUs using on-chip hardware ASTC decompression engine

QUALCOMM | Engineering Intern — Summer 2015 | San Diego, CA
Team: SoC Design
Mentor: Tony Flores • Manager: Alan Young

- Designed and verified new features for the Qualcomm debug subsystem for next-gen Qualcomm CPUs
- Automated the team's design flow process

QUALCOMM INDIA PVT. LTD. | Associate Engineer (Full-time) — July 2013 - May 2014 Team: Emulation Team, Bengaluru, India
Mentor: Sivashankar Madheswaran • Manager: Pavan Kumar Adepu

- Pre-silicon testing and verification for Qualcomm Snapdragon chips using FPGAs

QUALCOMM INDIA PVT. LTD. | Engineering Intern — Summer 2012
Team: Emulation Team, Bengaluru, India
Mentor: Sivashankar Madheswaran • Manager: Jaya Subramanian Sundaresan

- Developed Programmer's Hardware Trace (PHT) - a hardware module for analyzing trace signals over JTAG for fast debugging

INDIAN SPACE RESEARCH ORGANIZATION (ISRO) | Engineering Intern
Summer 2011| Ahmedabad, India Team: Space Applications Centre (SAC) Mentor: Jayesh Jayarajan • Manager: Rajiv Kumaran

- Built an FPGA-based Fire and Smoke Detection System through, as a part of 'Environmental control life support system for human space flight' by SAC, ISRO

ARTIFACTS

- DNNWEAVER: From High-Level Deep Neural Models to FPGAs | http://act-lab.org/artifacts/dnnweaver
- TABLA: An Accelerator Generator for a class of Machine Learning Algorithms | http://act-lab.org/artifacts/tabla

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TEACHING EXPERIENCE

Teaching Assistant

Course | ACT: Alternative Computing Technologies
Instructor | Prof. Hadi Esmaeilzadeh
Location | Georgia Institute of Technology

Teaching Assistant

Course | Computer Architecture: Processor Design
Instructor | Prof. Hadi Esmaeilzadeh
Location | Georgia Institute of Technology

Teaching Assistant/Lead Organizer

Course | Arch-Whisky: A Weekly Computer Architecture Seminar
Instructor | Prof. Hadi Esmaeilzadeh
Location | Georgia Institute of Technology