

MITCHELLE RASQUINHA

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M.S. Electrical & Computer Engineering * Georgia Institute of Technology * Fall 2007 * GPA 3.4 *
B.S. Electronics & Telecommunications * *PESIT*, Visvesvaraya Technological University * GPA 3.8

Goal: Computer engineering major application for **Full time Employment [Jan 2012]** in Computer Architecture

Masters Thesis: *An Energy Efficient Cache Design Using Spin Torque Transfer RAM*

The thesis evaluates the feasibility of using STT-RAM, a novel memory technology for caches in modern processors. It also proposes optimizations for minimizing the energy consumption of such a cache.

Interest: Heterogeneous many core architectures, On-chip networks, performance analysis, memory system optimization, memory system design, modelling and simulation

Academic Projects

Computer Architecture (Georgia Institute of Technology)

- Analytical models for evaluating the impact of 3D system integration
- Analysis of address mapping schemes in multiple memory controller multiple core environments and their effect on standard page mapping algorithms
- Analysis on the scope of adaptive routing schemes in multiple memory controller environments with different memory mapping schemes
- Author of the IRIS network simulator in the Manifold simulation infrastructure
- Design and Micro-architecture Optimization of Spin Torque Transfer RAM based cache memory
- Implemented a VIVT Instruction Cache simulation model in verilog.
- Implemented a simulation model of the Tomasulo Algorithm using C++.
- C++ based MOESI cache simulator

Multiprocessor Interconnection Networks

- Authored a term paper on Performance Analysis of High Radix Routers in On-Chip Networks.
- Built a simulation model for a four port wormhole switched router.

Compilers and Interpreters

- Implemented a front end for the Lua scripting language. Implemented optimization passes within LLVM.

Advanced VLSI

- Simulated a SRAM (16x16) memory array using Cadence of clock frequency of 2GHz

High Performance Parallel Computing

- Implemented single core optimizations and cache-based tuning for dense matrix multiplication.

Course Work: *Advanced Computer Architecture, Advanced VLSI, High Performance Parallel Computing, Distributed Computing, Multiprocessor Interconnection Networks, Compilers and Interpreters.*

Work Experience

Sandia National Laboratory - Intern at Albuquerque, NM (Aug 2011 to present)

- Implementing a cycle accurate network model for the SST framework. SST is a simulation infrastructure for evaluating large scale systems. A key goal of the project is to provide the ability to explore innovations in highly concurrent systems where the ISA, microarchitecture, and memory interact with the programming model and communications system.

Research Assistant at Computer Architecture and Systems Laboratory, Georgia Institute of Technology (Aug 2008 to present)

- Investigating issues in on-chip and 3D interconnects, modeling and simulation of multicore architectures, and architectural impact of novel memory technologies.
- Added a cycle accurate network on chip model to the Manifold, many core project. The Manifold project is a C++ based simulation infrastructure for evaluating many-core and scalable system architectures.

Intel Corporation Intern at Oregon CPU Architecture Team(May 2009 to July 2009)

- Modeling and simulation tool chain development for for graphics micro-architecture studies.

Intel Corporation Intern at Mobility Group, Bangalore, India(Jan 2009 to April 2009)

- Analysis of gaming workloads for future processor design.

Tavant Technologies, Senior Software Engineer at Bangalore, India

- Developed web based application for mortgage client using J2EE. Responsible for backend and business layer development from design to deployment.

Publications

- Michelle Rasquinha, Minhaj Hassan, Kwanyeob Chae, William Song, Minki Cho, Saibal Mukhopadhyay and Sudhakar Yalamanchili, “Exploiting the Long-term Advantages of 3D Integration: A System-Driven Approach”, *Interconnect Focus Center Annual Review 2010 (Poster Session)*.
- Michelle Rasquinha, Minhaj Hassan and Sudhakar Yalamanchili, “Impact of Adaptive Routing with Multiple Memory Controllers”, Currently under Review for a conference.
- Minhaj Hassan, Dhruv Choudhary, Michelle Rasquinha and Sudhakar Yalamanchili, “Managing Physical Address Spaces in Multiple Memory Controller Environments”, Currently under Review for a conference.
- Michelle Rasquinha, Dhruv Choudhary, Subho Chatterjee, Saibal Mukhopadhyay and Sudhakar Yalamanchili, “An Energy Efficient LLC Cache Design Using Spin Torque Transfer (STT) RAM”, *International Symposium on Low Power Electronics and Design (ISLPED) 2010*.
- Subho Chatterjee, Michelle Rasquinha, Saibal Mukhopadhyay and Sudhakar Yalamanchili, “A Methodology for Robust, Energy Efficient Design of Spin-Torque-Transfer RAM Arrays at Scaled Technologies”, *International Conference on Computer-Aided Design (ICCAD) 2009*.
- Subho Chatterjee, Michelle Rasquinha, Saibal Mukhopadhyay and Sudhakar Yalamanchili, “A Scalable Design Methodology for Energy Minimization of STTRAM: A Circuit and Architecture Perspective”, *Transactions on Very Large Scale Integration (VLSI) Systems 2009*.

Programming Language And Tools

Standard Cell Design using Cadence Virtuoso(Layout and Hspice simulation)

C, C++, Verilog, Perl, Java

x86 assembly, MIPS, Keil Cross Compiler, Python, Modelsim, Matlab, Yacc/Bison Also worked with various micro-architectural simulators. Operating Systems: Linux, Microsoft Windows Experience working with J2EE platform: Weblogic, EJB, JRules, Hibernate, Oracle DB

Communication Skills

Good interpersonal and communication skills, actively participated in debates.

References will be made available on request.